IN THE SPECIFICATION

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please replace the paragraph starting on page 4, line 19 with the following paragraph:

FIG. 2 pulse 2A shows a conventional data signal applied, for example, to the input 20 of the buffer circuit 10 to provide an output pulse on the buffer output 30 which would then be applied to the associated external pin of the IC containing the buffer 10. ~~FIGS.~~ Pulses 2B, 2C and 2D show similar data signals applied to the inputs 22, 24 and 26 of the buffers 12, 14 and 16. If, as is shown in ~~FIGs.~~ FIG. 2 pulses 2A to 2D, the H-L transitions (i.e., trailing edges) of the data signals coincide and thus the buffers 10 to 16 are switched simultaneously, then a ground bounce (i.e., a rise in the source voltage VSS immediately following the H-L transitions) can occur as shown in ~~FIG.~~ pulses 2E. Conversely, if the L-H transitions (i.e., leading edges) of the data signals coincide, then a power droop in the voltage VDD immediately following the L-H transitions can occur as shown in ~~FIG.~~ pulse 2F. If the L-H transitions occur a time T1, then the power droop occurs a short time afterwards at time TD. If the H-L transitions occur at a time T2, then the ground bounce occurs a short time afterwards at time TB.

Please replace the paragraph starting on page 6, line 12 with the following paragraph:

As will be appreciated, as the number of buffers which can switch simultaneously in the same direction increases, then the number of pairs of power and ground pins required will increase. In the example of FIG. 1, if analysis of the circuit has shown that the four buffers connected to the same VDD/VSS pair results in the ground bounce and/or power droop shown in ~~FIGs. 2A-F~~ pulses 2A-2F then more than one pair of power/ground pins would be required for this group. The analysis, in turn, results either in a limitation in the number of pins that can be used for transferring data from the IC or requires an increase in the size of the IC to accommodate the extra pins required.

Please replace the paragraph starting on page 12, line 2 with the following paragraph:

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a schematic diagram of a conventional array of input/output switching buffers;

~~FIGs. 2A-F are diagrams~~ FIG. 2 is a diagram showing the relationship between the input data switching pulses for the I/O buffers of FIG. 1 and power droop and ground bounce pulses;

FIG. 3 is a schematic diagram of an integrated circuit according to a preferred embodiment of the present invention, connected through transmission lines to a receiving integrated circuit;

FIG. 4 is a schematic diagram of an SSO doubler of the integrated circuit of FIG. 3;

FIG. 5 is a schematic diagram of a transition checking circuit as used in the SSO doubler of FIG. 4;

FIG. 6 is a schematic diagram of a control circuit of the SSO doubler of FIG. 4; and

FIG. 7 is a schematic diagram of a demultiplexer circuit for the receiving integrated circuit of FIG. 3.